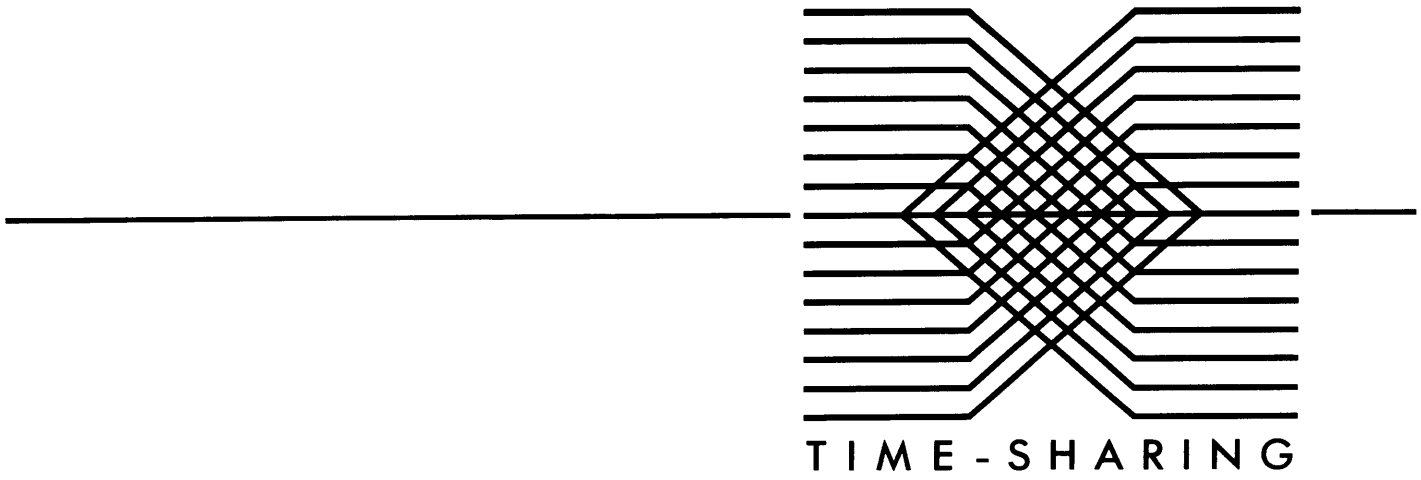

CONTROL DATA® 3300/3500 Computer Systems Equipment Bulletin

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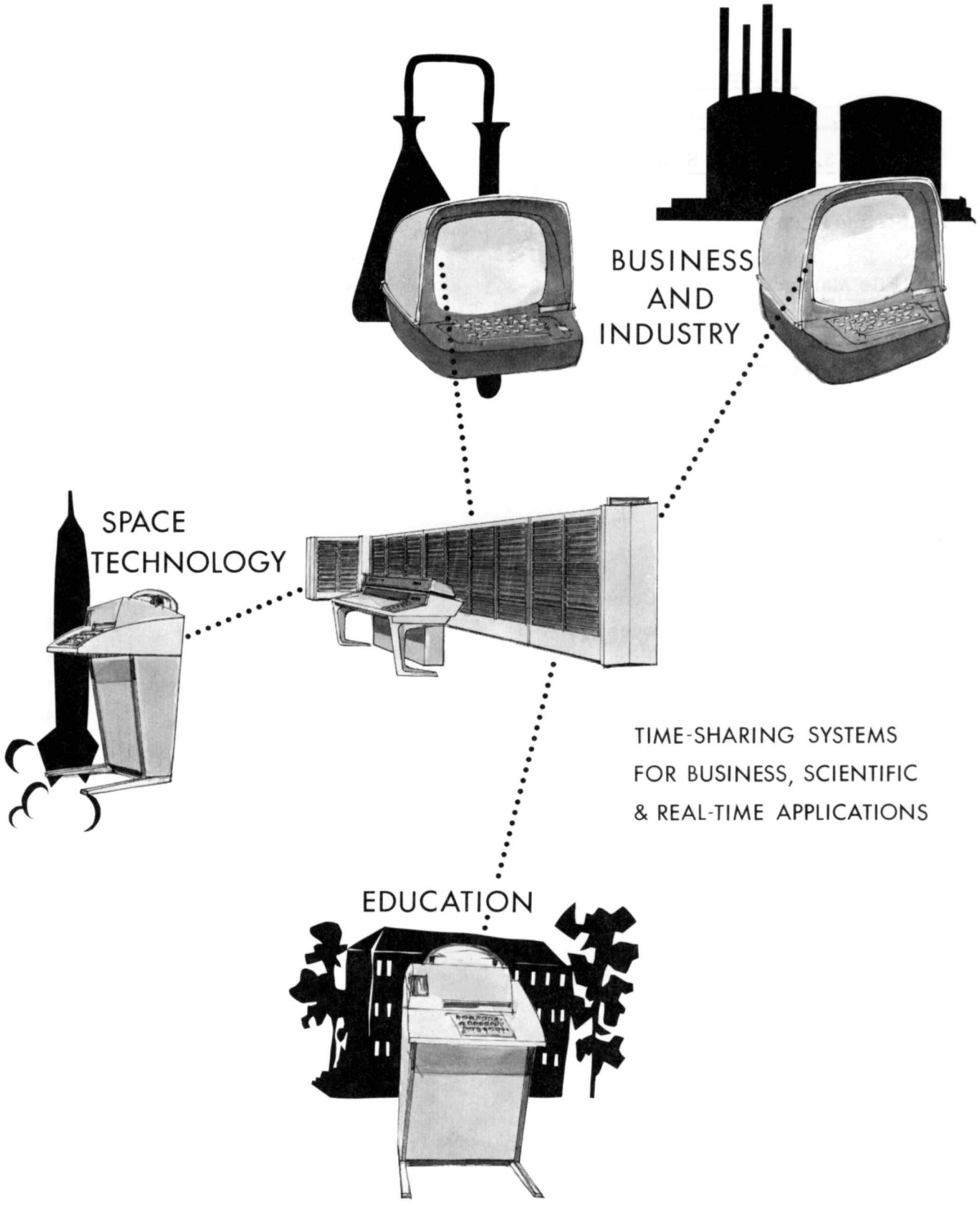
BUSINESS
AND
INDUSTRY
SPACE
TECHNOLOGY
TIME-SHARING SYSTEMS
FOR BUSINESS, SCIENTIFIC
& REAL-TIME APPLICATIONS
EDUCATION

1. INTRODUCTION

Control Data's 3000 Series Computer Systems is again expanded to include the CONTROL DATA* 3300 and 3500 Data Processing Systems. These computers provide high performance time-sharing with multiprogramming features to satisfy the present and future needs of business and scientific users.

The 3300 and 3500 Computer Systems provide a choice of two extremely powerful, efficient, and versatile data processing systems, surpassing the performance of any other computer of comparable cost. Computations per dollar per second are kept at a maximum through optimum hardware usage by advanced time-sharing techniques and comprehensive software systems.

The time-sharing and multiprogramming features of these systems enable users to enter many programs and receive processed results without the delays incurred in single job batch processing systems. This not only reduces turnaround time but also provides a user with a considerable saving in computer usage and personnel time. Multiprocessing of programs further enhances system performance when additional central processors are integrated into a total system.

New software systems take full advantage of the time-sharing and multiprogramming capabilities of the 3300 and 3500 systems by including the Multiple Access, Shared Time, Executive Routine (MASTER) operating system, Real-Time SCOPE (including all of the capabilities of the present 3200 SCOPE), Disk SCOPE, File Manager, and Mass Storage Input/Output (MSIO) system. A synopsis of each of these systems is included in Section 3.

The 3300 and 3500 computers provide all of the salient features found in the 3200 system and also furnish business and scientific users with the following features:

- Large memory capacity - A minimum core memory of 8,192 twenty-four bit words (32,768 characters) can be augmented with additional storage modules to bring either system up to 262,144 words (1,048,576 characters). Mass storage devices such as drums and disks are particularly suited for these systems.

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- Multiprogramming Module. This module provides dynamic storage allocation by relocating program instructions, data, and I/O in magnetic core memory. It also provides memory expansion capability to 262,144 words.
- Business Data Processing Module. This module provides the hardware necessary to execute business oriented instructions. It also contains its own translation and control logic.

Figure 2-1. 3300 Computer System Console

3. SOFTWARE SYSTEMS

MASTER (Multiple Access, Shared Time, Executive Routine)

MASTER is an advanced time-sharing operating system for 3300 or 3500 computers equipped with the multiprogramming option. It provides efficient batch processing by overlapping I/O functions with compute tasks from single or multiple jobs, and simultaneously provides conversational computing facilities for jobs submitted from multiple consoles. Background peripheral processing routines are provided by the system for reading, printing, and punching of job associated files. I/O equipment and files are assigned to programs as they are required.

Extremely fast response time is achieved by dynamic memory and I/O equipment assignment. Efficiency is kept at a maximum using this form of dynamic allocation. Manipulation of the particular installation parameters permits shifting of emphasis on multiple access to batch processing or vice-versa.

The multiprogramming option and its inherent memory protection features enables core memory to be loaded with individual jobs and operating system tasks to its maximum capacity. Dynamic assignment is made either at call time or when a task first references a specific block of memory.

Tasks are internally processed on a priority basis. Normal jobs are grouped according to their job class and provision is made for immediate attention on emergency jobs.

REAL-TIME SCOPE

Real-Time SCOPE includes all of the features provided by 3200 SCOPE and also provides a complete batch processing operating system for a 3300 or 3500 Computer System. This operating system provides priority interrupt handling and time-sharing between a background program and batch processing on an interrupt determined basis. Serially stacked jobs are processed with an absolute minimum of operator intervention.

One program may be loaded into core storage while stacked jobs are being processed on a time-shared basis. This program may be a real-time job and can receive program control on demand and retain it until its needs are satisfied. A program requiring a fast response at discrete time intervals is ideal in this sit-

uation since the system provides priority interrupt handling. Real Time SCOPE allows the user to reserve one or two channels for high priority work and any interrupt on the reserved real-time channels is granted priority.

Time-sharing allows an overlap of I/O functions thus increasing the efficiency of the computer. A program that is input/output bound functions very well as a background program.

MSIO (Mass Storage Input/Output System)

This system provides a user with a basic file oriented input/output package for operating with mass storage devices and magnetic tape units. MSIO operates under Real-Time SCOPE and performs I/O operations on mass storage devices as well as standard peripheral units. MASTER also utilizes MSIO in its I/O system.

Some of the more important features of MSIO include:

- Allocate and protect permanent files on mass storage devices and magnetic tape.
- Increase and decrease the file allocation on mass storage devices.
- Generate and process equipment and file labels for mass storage devices and files.
- Initialize and terminate file processing with the Open and Close internal program requests.
- Provide for sequential, sequential with linkage, or random file processing.
- Read and write file records from mass storage and magnetic tape devices with the Read and Write internal program requests.
- Process variable length and fixed length record blocks on mass storage devices and magnetic tape.
- Process fixed and variable length logical records.
- A Seek Address key, which is set and retrieved by the internal program request Locate, is used to specify the location of a block and logical record on a mass storage or magnetic tape device.
- Inform the user as to the status of his file through the internal Status request. Both hardware and logical conditions such as error indications are furnished to the user.
- Search for a logical record in a file on a mass storage device with the internal program requests Look and Search. The Look request scans the file from a specified record; the Search request performs a bisecting scan of the file.
- Add, delete, and replace logical records on mass storage devices with the linkage file processing.
- Provide a set of utility routines to load, reorder, and reallocate files contained on mass storage devices.

File Manager

The File Manager system operates in conjunction with MSIO to provide a central repository for all data accruing in a particular data center. Data is organized into program or data files by this system to satisfy the file handling requirements of both business and scientific users.

File Manager is organized around a language accessible to users at remote consoles and local operator consoles. A user at a console may enter data or programs directly into mass storage files, retrieve data in source or report form, and submit requests for job executions. Programs running under the system also have access to file handling subroutines via direct calls rather than through the language processor.

When operating with Real-Time SCOPE, catalogue functions, file manipulation functions, and functions related to file records are provided by the File Manager system and executed in the background of stack job processing. Program executions requested through File Manager and other file handling functions are queued to Real-Time SCOPE for execution in the job stack mode.

Under the MASTER system, File Manager operations are time-shared in the same manner as other programs.

Disk SCOPE

The Disk SCOPE system provides a user with a complete operating system for his installation using disk packs in lieu of magnetic tape units. This system has all of the features found in the magnetic tape SCOPE plus providing the capability of simulating magnetic tape units on disk drives. The user may execute programs written to perform I/O operations on magnetic tapes utilizing disk drives rather than magnetic tape units.

4. MULTIPROGRAMMING CONCEPTS

Multiprogramming in the 3300 and 3500 Computer Systems enables the instructions of many programs to be sequentially executed by controlled time-sharing operations within a processor. With the Control Data Multiprogramming Modules, throughput is very high due to efficient use of hardware and optimum program scheduling. This feature is very desirable at installations where numerous jobs are run and computing time must be kept at a minimum. Systems equipped with the relocation feature can compute many programs on a time-shared basis or be switched into the 3200 mode and process jobs according to control card job assignments.

EXECUTIVE MODE

A system equipped with relocation hardware and operating in the Executive Mode functions in either the Monitor State or the Program State.

Monitor State

The Monitor State is the initial operating state of a master-cleared processor. The processor also reverts to this state if interrupted for any condition. All instructions may be executed in the Monitor State.

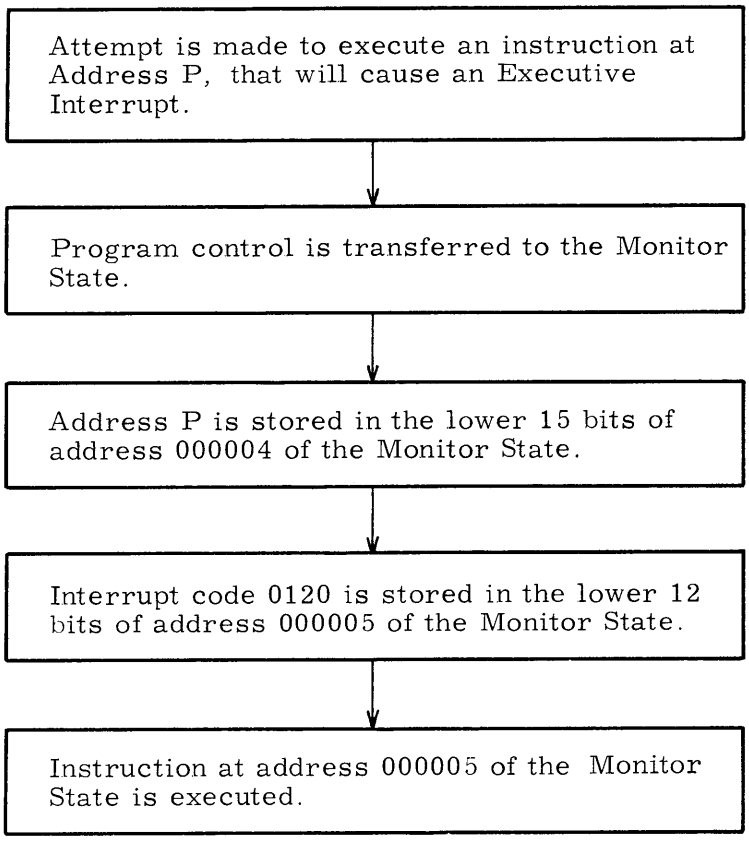
Program State

The Program State permits all but the following instructions to be executed:

1. A Halt instruction (00.0)
2. Any of the block instructions (71-77), or
3. An inter-register transfer instruction that attempts to alter registers 00 through 37 of the register file.

If an attempt to execute one of these instructions occurs, an Executive Interrupt is generated and operating control is transferred back to the Monitor State. The Executive Interrupt is not masked and the interrupt system need not be enabled to recognize the interrupt when it occurs. Upon recognition, the Executive Interrupt transfers program control to the Monitor State. The instruction that caused the interrupt is not executed. The following flow chart describes the sequence of events involved when an Executive Interrupt occurs.

EXECUTIVE INTERRUPT SEQUENCE



RELOCATION

A 3300 or 3500 central processor can access up to 262,144 words of core storage when the relocation option and appropriate storage modules are present in the system. This is accomplished by augmenting the basic 15 bit address P with with a 3-bit state number. The state number along with a portion of the 15-bit address becomes the direction path into a relocation path. From the relocation file the correct page address is obtained for actual memory addressing.

Page Structure

Each page of memory is assigned 2,048 absolute memory locations. A fully expanded system contains 128 of these pages. Individual pages may be subdivided into four partial pages. A 1/4 page consists of 512 address locations. Programs may be allocated full pages, 3/4 page, 1/2 page or 1/4 page of memory.

To facilitate addressing with the paging scheme, a word organized core matrix is used. This core matrix, called the Page Index File, is referenced by a program during a memory reference to obtain the physical page address or partial page address and provide memory protection.

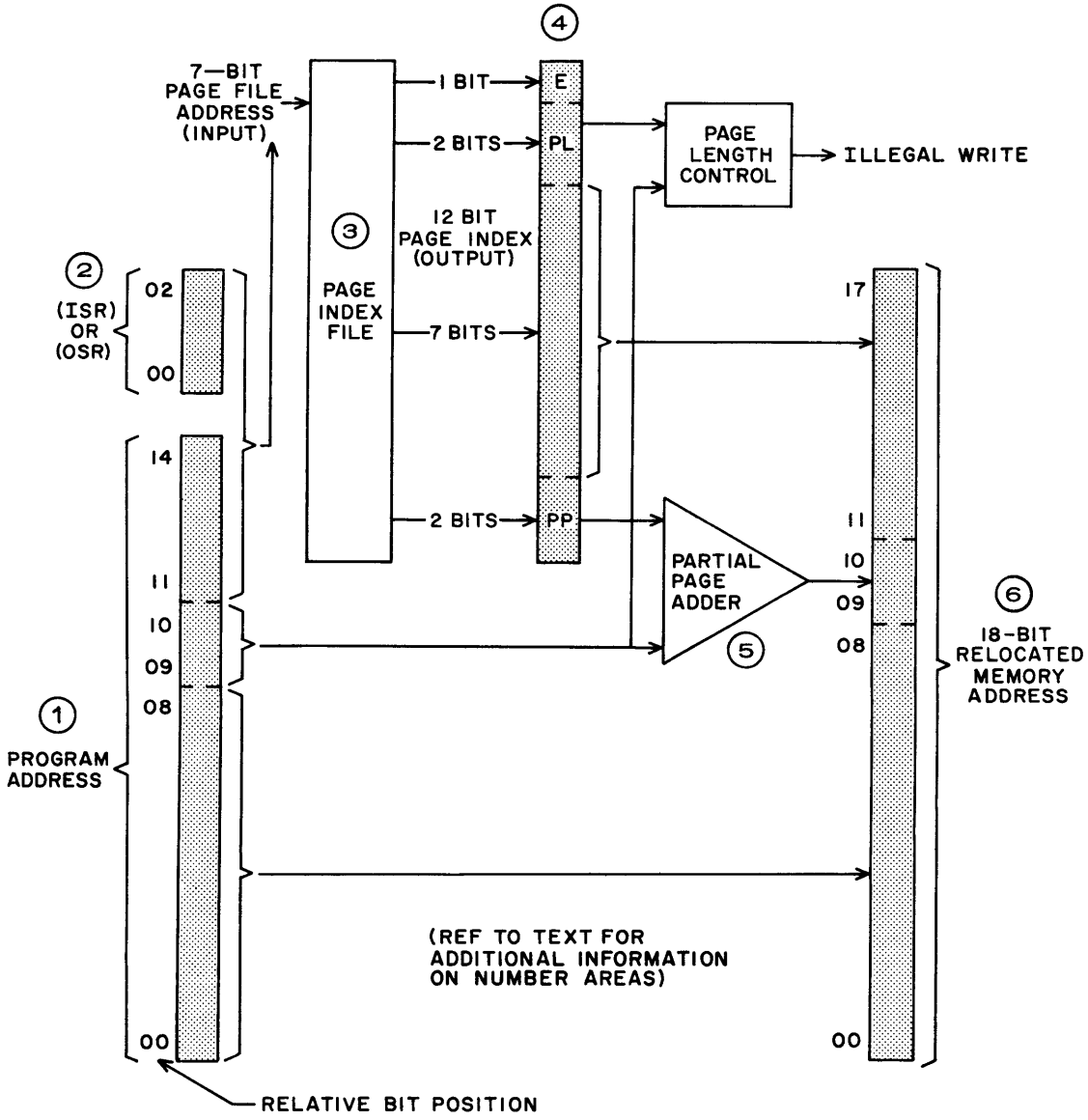


Figure 4-1. Address Relocation Process

Address Relocation

Figure 4-1 illustrates address bits at various stages of the relocation process. Those portions of the diagram accompanied by circled numbers are further described in the following numbered paragraphs.

① Program Address and Program Address Group

Any program executed by a 3300 or 3500 Computer System is processed within the confines of a 15-bit program address structure. These 15 bits define the program or operand address related to the routine or subroutine being processed at a given instant. Figures 4-2 and 4-3 illustrate the significance of these bits in the instruction words for both word addressing and character addressing.

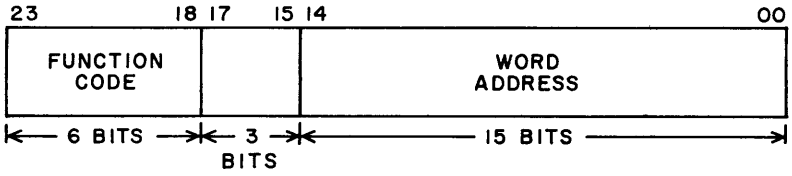


Figure 4-2. Word Addressing

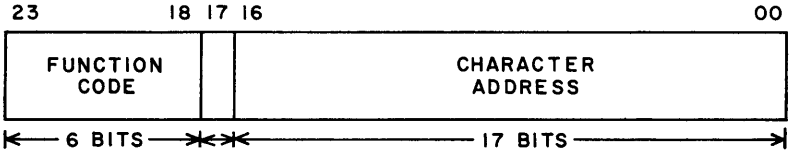


Figure 4-3. Character Addressing

The 15 bits used in word addressing define an absolute address assignment ranging from 00000 to 77777_8. Any program or group of programs within this range of addresses which can be compiled and loaded without conflicting addresses can be considered part of a program address group. Figure 4-4 is illustrative of a program address group consisting of five non-conflicting programs.

A program address group may be considered apart from the physical memory structure since it is a group of sequentially numbered addresses representing one or more programs within 32,768 words of storage and not a discrete physical device. Many program address groups may be contained in storage; however, eight such groups are used in the 3300 and 3500 Computer Systems to best optimize the memory system.

② Instruction State Register (ISR) and Operand State Register (OSR)

The ISR and OSR define the specific program address group currently being accessed by a processor. The program address group being referenced for instructions and operands can assume any one of eight discrete values by modifying the contents of these single digit registers. By transferring dissimilar numbers into these registers, instructions and operands may reference different program address groups.

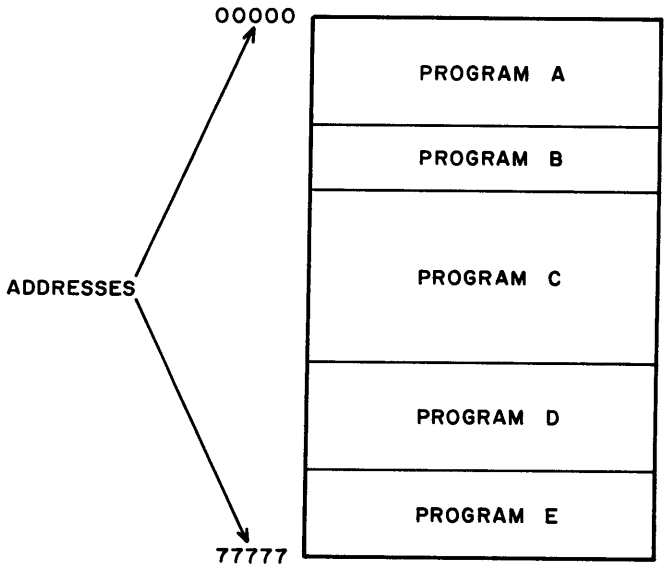


Figure 4-4. Program Address Group

The contents of these registers can only be changed by the Executive routine in the Monitor State.

The program address group that is currently valid for memory references is selected by the contents of the ISR or OSR. The following table describes the selecting conditions.

Operational State of the Processor	Instructions Referenced With:	Operands Referenced With:
Initial Monitor State	Zero	Zero
Monitor State and 55.4 (relocate to operand state) instruction executed	Zero	Contents of OSR
Transition from Monitor State to Program State	Contents of ISR	Contents of ISR*
Program State and 55.4 (relocate to operand state) instruction executed	Contents of ISR	Contents of OSR
Program State and 55.0 (relocate to instruction state) instruction executed	Contents of ISR	Contents of ISR
Any interrupt condition to Monitor State	Zero	Zero

*Transition from Monitor State to Program State does not change the operand address mode.

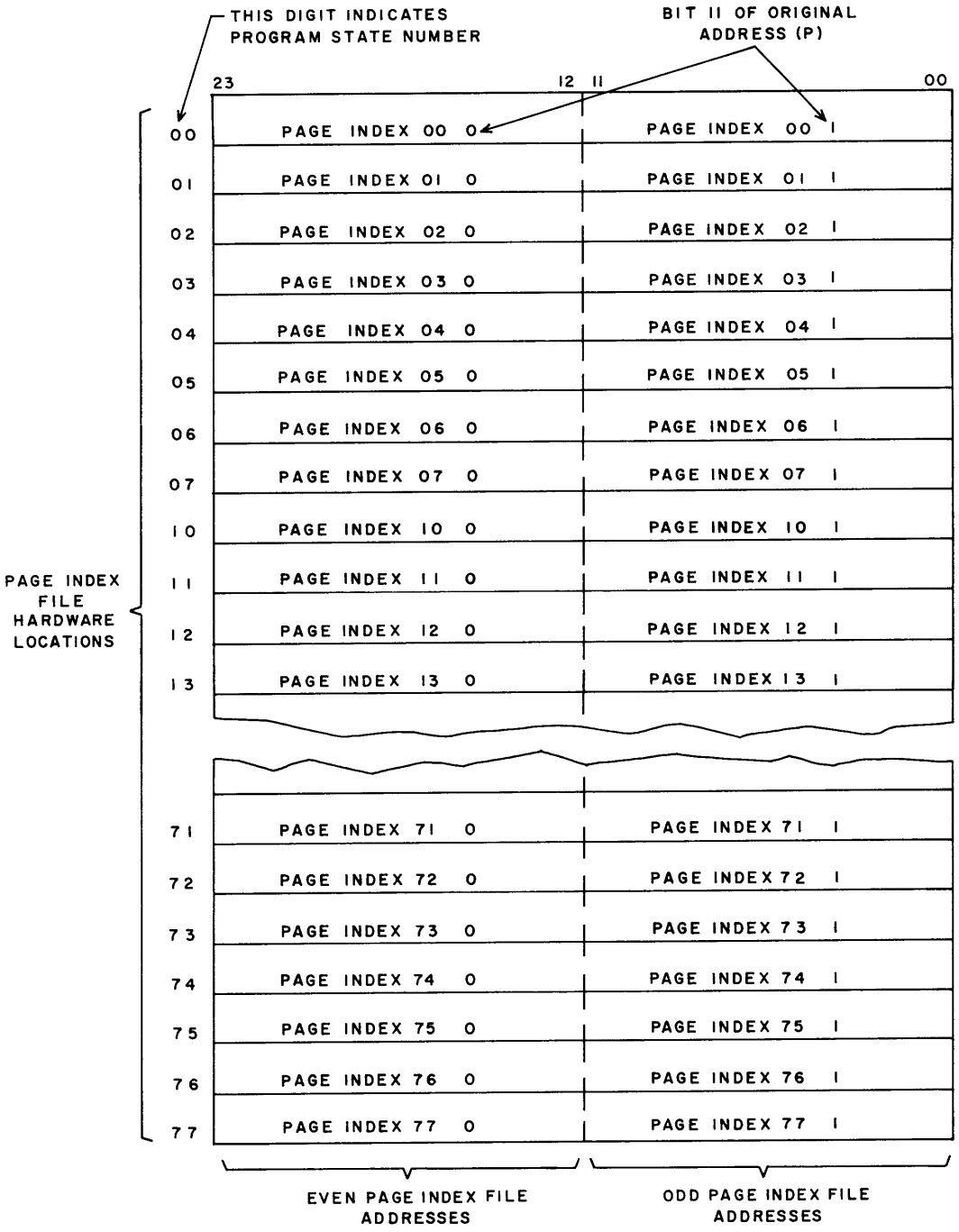


Figure 4-5. Page Index File Address and Hardware Structure

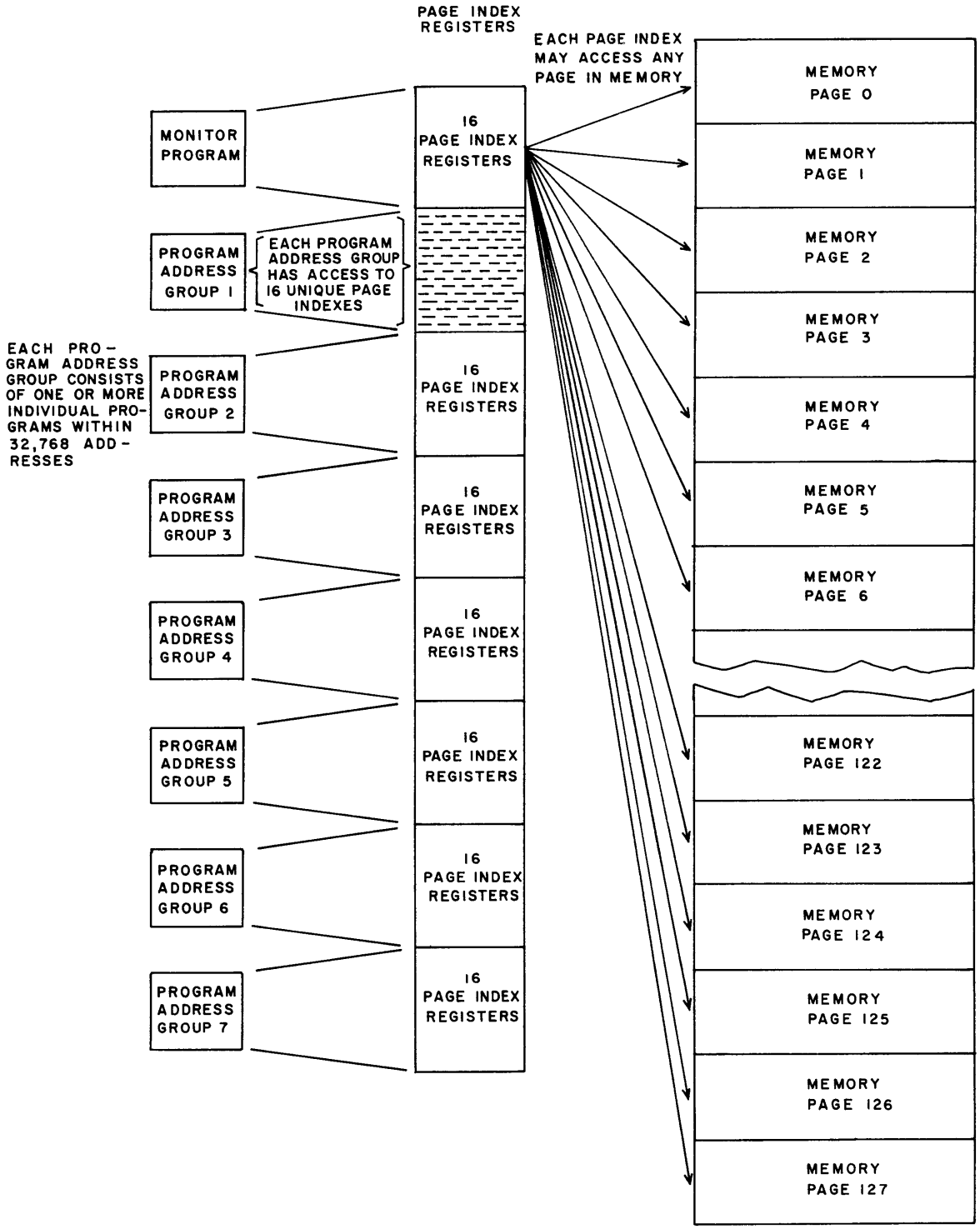


Figure 4-6. Relocation System Illustrating Memory Protection with Fully Expanded Memory (262K)

③ Page Index File

The Page Index File is functionally divided into eight distinct reference areas. One area is associated with each of eight possible numbers appearing in the ISR and OSR. Because of this direct relationship, each of the eight program address groups is permanently assigned a reference area in the Page Index File.

Each of the eight reference areas within the Page Index File consists of sixteen 12-bit Page Index Registers. This provides each of the program address groups exclusive use of 16 of these registers. By using the upper four bits of the program address for direction to the respective Page Index Registers, a direct and sequential relationship is established between the addresses in a program address group and a specific set of 16 Page Index registers. The Page Index File is actually constructed of sixty-four 24-bit Page Index registers with dual 12-bit indexes. Only one of the 12-bit indexes is used during any specific reference.

Figure 4-5 depicts the Page Indexes within the Page Index File and Figure 4-6 illustrates the relationship between program address groups, Page Index File, and a fully expanded core memory.

Bit 11 of the original 15-bit address determines which of the two page indexes at the Page File location will be used. Figure 4-7 shows a specific page index being referenced.

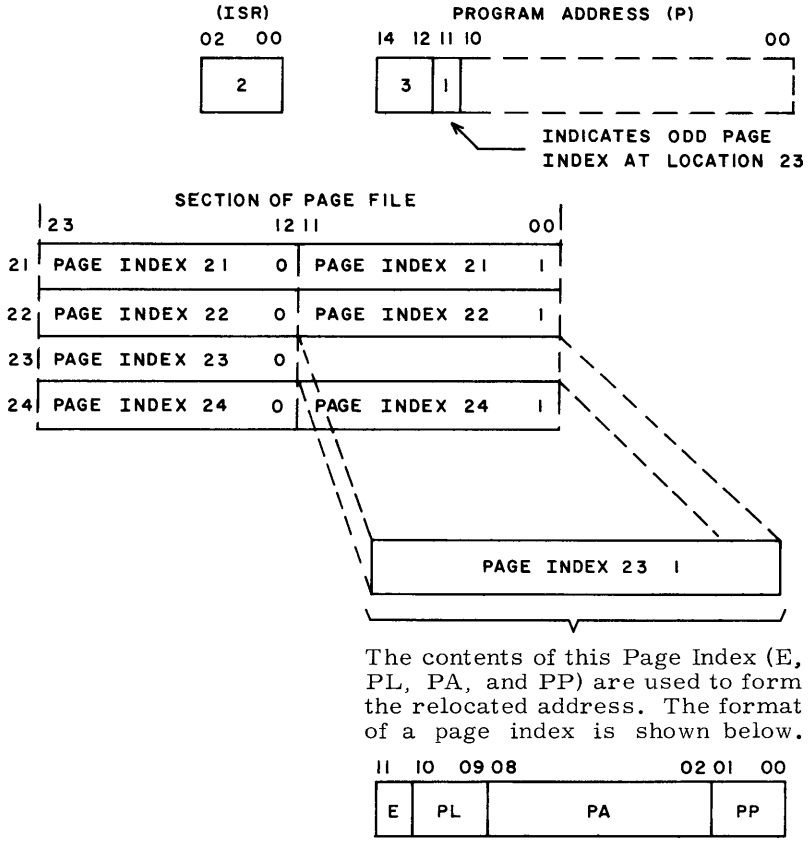


Figure 4-7. Example of Page Index Referencing

④ Page Index

Each page index has the same basic format. The significance of each designator during the relocation process is described below. Figure 4-8 shows the format for a page index while Figure 4-9 shows a view of the display panel on the relocation chassis.

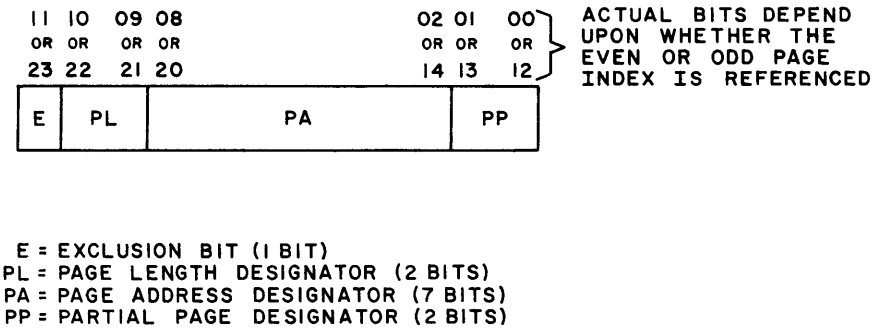


Figure 4-8. Page Index Format

E - Exclusion bit

This designator may have one of three meanings:

1. If E = "0", the quantity expressed by PA defines a page where either reading or writing is permitted.

2. If E = "1", and PL, PA or PP is a quantity other than zero, PA defines a page address where only reading is permitted.

3. If E = "1" and PL, PA, and PP are all equal to zero, an unaddressable page is defined and an Illegal Write interrupt is generated by the Page Index File.

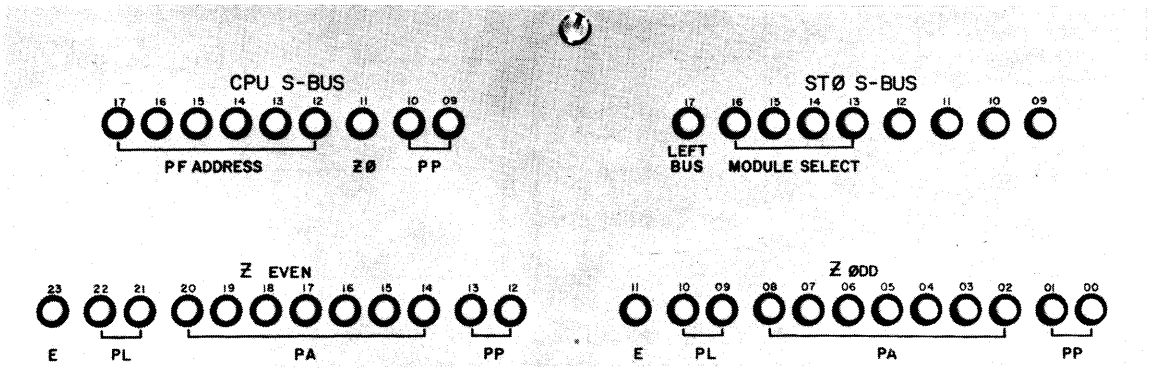


Figure 4-9. Relocation Chassis Display Panel

PA - Seven bits are used to define the actual memory module being referenced. As stated earlier in this manual, there may be 128 segmented pages in a 3300 or 3500 system with 262,144 words of core storage. Each page has a unique page address and addresses 000 through 177_8 define all of the possible pages.

A 3300 or 3500 system with a fully expanded storage network has two address busses. Each bus has access to 131,072 words of the total 262,144 storage words. The uppermost bit of PA (bit 17 in the relocated address) determines which bus (right or left) is selected. This bit will be a "1" when the left bus is used and a "0" when the right bus is selected. Figure 4-10 depicts the bus address system.

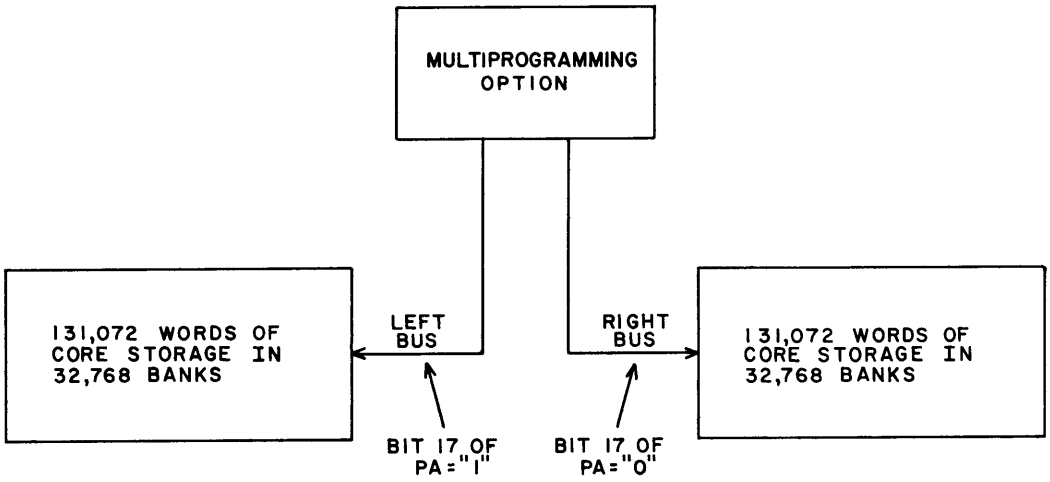


Figure 4-10. Storage Address Buses

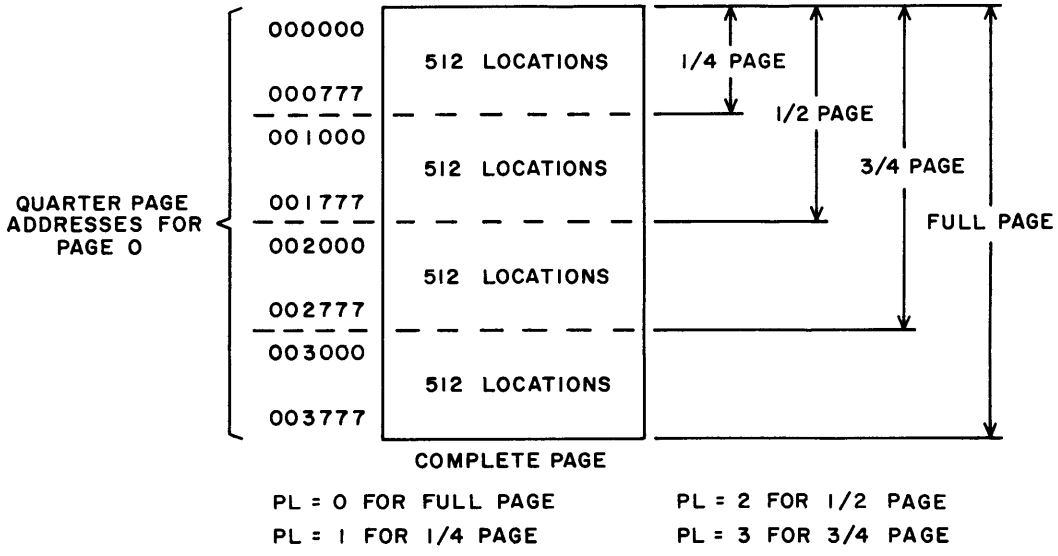


Figure 4-11. Page Length Subdivisions

PL - Each page has 2,048 memory locations and is subdivided into quarters of 512 locations each. The PL designator defines how many quarters of a page can be referenced; thus, a program is assigned the number of quarter pages it needs to reside in memory. Figure 4-11 illustrates the quarter sections of a page and the significance of the PL bits.

PP - The Partial Page designator defines the particular quarter page that will functionally serve as the starting point of the page. Example A (Figure 4-12) shows the quarter page referenced for each of the PP designators. The significance of the PP designator in selecting the respective quarter page for addressing is described below.

Example A

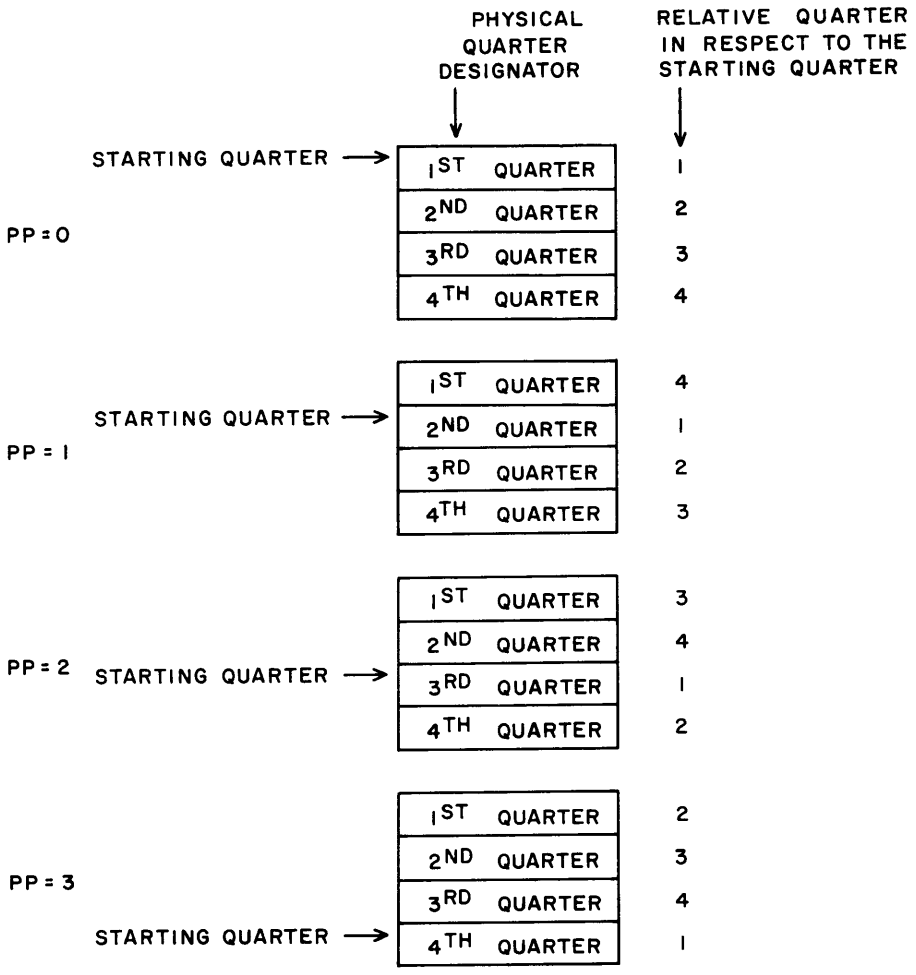


Figure 4-12. Quarter Page in Relation to PP Designator

If PP = 0, addressing begins in 1st relative quarter

If PP = 1, addressing begins in 2nd relative quarter

If PP = 2, addressing begins in 3rd relative quarter

If PP = 3, addressing begins in 4th relative quarter

⑤ Partial Page Adder

A special adder is used to combine the PP designator from the page index with bits 9 and 10 of the original address. The PP designator indicates in which quarter page addressing will begin in respect to the relative quarters as shown in Figure 4-12. Example B and Figure 4-13 show the actual quarter page in which addressing accurs for specific PL, PP, and bits 9 and 10 values.

Example B

PL = 0

PP = 1

Bits 9 and 10 = 2

Analysis: A full page (PL = 0) is allocated, the starting quarter (relative quarter 1) is the second physical quarter, and addressing begins in the third relative quarter, (fourth physical quarter).

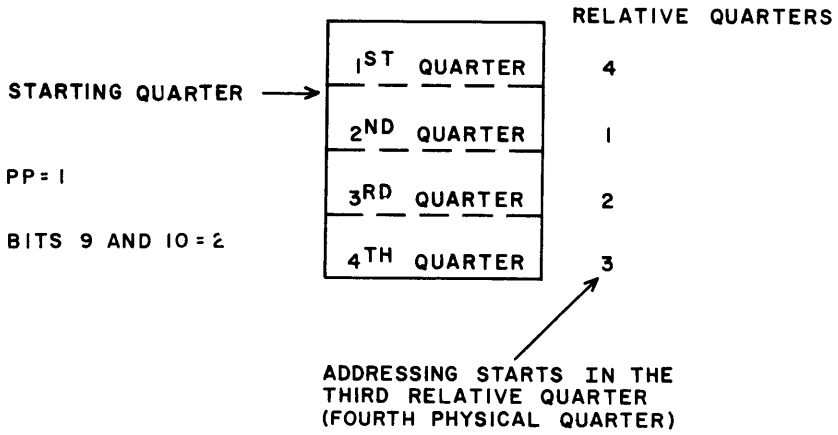


Figure 4-13. Starting Quarters versus Relative Quarters

It should be noted that if bits 9 and 10 of the original address specify a quarter page greater than that allocated by the PL designator for PL ≠ zero, an Illegal Write interrupt will occur. An example of this condition would be a 1/4 page allocated but bits 9 and 10 equal to 3, thus specifying an address in the fourth quarter.

⑥ Relocated Address

The 18-bit relocated address defines the actual core storage location being referenced.

The PA portion of the page index fills the upper seven bits of this address (S) bus to use and select the appropriate storage module. Bits 9 and 10 receive the output of the adder previously described and indicate the physical quarter page being referenced. The lower nine bits are unaltered from the original address and comprise the remainder of the relocated address.

Page Zero Consideration

If Page Index File address zero is referenced in either the Program or Monitor state, the PA and PP designators for this page index will always be zero. As a result of this condition, page zero, which encompasses addresses 000000 through 003777, can be accessed and used for storing the Autoload and Autodump routines. The Autoload routine is contained in addresses 003700 through 003737 and the Autodump routine is stored in addresses 003740 through 003777.

INSTRUCTIONS

The following pages list the instructions for the 3300 and 3500 Computer Systems. Business data processing, floating point, and 48-bit precision multiple and divide instructions are trapped if the hardware options are not present in a system. Some of the new instructions require the computer to be in either the Monitor or Program State of Executive Mode or an Executive or Illegal Write interrupt will occur.

3300 AND 3500 INSTRUCTION LIST

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
ACI	77.54		$(A_{00-02}) \rightarrow$ Channel Index Register A TO CHANNEL INDEX REGISTER
ADA, I	30	m, b	Add (M) to (A) → A
ADAQ, I	32	m, b	Add (M, M + 1) to (AQ) → AQ
	66*		Conversions and translations for business data processing
ADM	67.0*	A, Ba, N1, C, Bc, N2	Add
AEU	55.6		$(A) \rightarrow E_U$
AIA	53.(0 + b) 4	b	Add (A) to $(B^b) \rightarrow A$
AIS	77.664		$(A_{00-02}) \rightarrow$ Instruction State Register (ISR) A TO INSTRUCTION STATE REGISTER
ANA	17.6	y	y ∧ (A) → A, no sign extension
ANA, S	17.4	y	y ∧ (A) → A, sign of y extended
ANI	17.1-3	y, b	$y \wedge (B^b) \rightarrow B^b$
ANQ	17.7	y	y ∧ (Q) → Q, no sign extension
ANQ, S	17.5	y	y ∧ (Q) → Q, sign of y extended
AOS	77.660		$(A_{00-02}) \rightarrow$ Operand State Register (OSR) A TO OPERAND STATE REGISTER
APF	77.64	w	$(A_{00-11}) \rightarrow$ Page File A TO PAGE FILE
AQA	53.04		Add (A) to (Q) → A
AQE	55.7		$(AQ) \rightarrow E_U E_L$
AQJ, EQ	03.4	m	If (A) = (Q), RNI @ m, otherwise RNI @ P + 1
AQJ, GE	03.6	m	If (A) ≥ (Q), RNI @ m, otherwise RNI @ P + 1
AQJ, LT	03.7	m	If (A) < (Q), RNI @ m, otherwise RNI @ P + 1
AQJ, NE	03.5	m	If (A) ≠ (Q), RNI @ m, otherwise RNI @ P + 1
ASE	04.6	y	If y = (A), RNI @ P + 2, otherwise RNI @ P + 1, lower 15 bits of A are used

*Trapped instruction if BDP module is not present in a system.

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
ASE, S	04.4	y	If y = (A), RNI @ P + 2, otherwise RNI @ P + 1. Sign of y is extended
ASG	05.6	y	If (A) $\geq$ y, RNI @ P + 2, otherwise RNI @ P + 1
ASG, S	05.4	y	If (A) $\geq$ y, RNI @ P + 2, otherwise RNI @ P + 1. Sign of y is extended
ATD	66.3*	A, Ba, N1, C, Bc, N2	Translate ASCII to BCD
ATD, D	66.3*	A, Ba, DC, C, Bc, N2	Translate ASCII to BCD
AZJ, EQ	03.0	m	If (A) = 0, RNI @ m, otherwise RNI @ P + 1
AZJ, GE	03.2	m	If (A) $\geq$ 0, RNI @ m, otherwise RNI @ P + 1
AZJ, LT	03.3	m	If (A) $<$ 0, RNI @ m, otherwise RNI @ P + 1
AZJ, NE	03.1	m	If (A) $\neq$ 0, RNI @ m, otherwise RNI @ P + 1
CIA	77.55		Clear A and transfer contents of Channel Index Register $\rightarrow A_{00-02}$
CILO	77.511	x	Lockout external interrupt on masked channel(s) x, until channel(s) is Busy
CINS	77.3	ch	Interrupt mask and internal status to A
CLCA	77.512	x	Clear the specified channel but not external equipment CLEAR CHANNEL ACTIVITY
CMP	67.3*	A, Ba, N1, C, Bc, N2	Compare
CMP,D	67.3*	A, Ba, DC, C, Bc, N2	Compare
CON	77.0	x, ch	If channel ch is busy, reject instruction, RNI @ P + 1. If channel ch is not busy, 12-bit connect code sent on channel ch with connect enable, RNI @ P + 2

*Trapped instruction if BDP module is not present in a system.

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
COPY	77.2	ch	External status code from I/O channel ch to lower 12 bits of A, contents of Interrupt Mask Register to upper 12 bits of A, RNI @ P + 1
CPR, I	52	m, b	(M)> (A), RNI @ P + 1 (Q) > (M), RNI @ P + 2 (A) $\geq$ (M) $\geq$ (Q), RNI P + 3 } (A) and (Q) are unchanged
CTI	77.75		Set Type In } Beginning character address must be preset in location 23 of register file and last character address + 1 must be preset in location 33 of the file
CTO	77.76		Set Type Out
CVBD	66.1	A, Ba, N1, C, Bc, N2	Convert binary to BCD
CVDB	66.0	A, Ba, N, C, Bc	Convert BCD to binary
DTA	66.2*	A, Ba, N1, C, Bc, N2	Translate BCD to ASCII
DTA, D	66.2*	A, Ba, DC, C, Bc, N2	Translate BCD to ASCII
DINT	77.73		Disables interrupt control
DVA, I	51	m, b	(A) $\div$ (M) $\rightarrow$ A, remainder $\rightarrow$ Q
DVAQ	57	m, b	(AQE) $\div$ (M, M + 1) $\rightarrow$ AQ and remainder with sign extended to E. Divide fault halts operation and program advances to next instruction
EAQ	55.3		$(E_U E_L) \rightarrow AQ$
ECHA	11.0	z	z $\rightarrow$ A, lower 17 bits of A are used
ECHA, S	11.4	z	z $\rightarrow$ A, sign of z extended
EDIT	64.4*	A, Ba, N1, C, BC, COBOL	Edit

*Trapped instruction if BDP module is not present in a system.

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
EINT	77.74		Interrupt control is enabled. Allows one more instruction to be executed before interrupt
ELQ	55.1		$(E_L) \rightarrow Q$
ENA	14.6	y	Clear A, enter y
ENA,S	14.4	y	Clear A, enter y, sign extended
ENI	14.1-3	y,b	Clear B^b, enter y
ENQ	14.7	y	Clear Q, enter y
ENQ,S	14.5	y	Clear Q, enter y, sign extended
EUA	55.2		$(E_U) \rightarrow A$
EXS	77.2	x,ch	Sense external status if "1" bits occur on status lines in any of the same positions as "1" bits in the mask, RNI @ P + 1. If no comparison, RNI @ P + 2
FAD,I	60	m,b	Floating point addition of (M, M + 1) to (AQ) → AQ
FDV,I	63	m,b	Floating point division of (AQ) by (M, M + 1) → AQ. Remainder with sign extended to E
FMU,I	62	m,b	Floating point multiplication of (AQ) and (M, M + 1) → AQ
FRMT	64.4*	A, Ba, N1, C, BC	Format
FSB,I	61	m,b	Floating point subtraction of (M, M + 1) from (AQ) → AQ
HLT	00.0	m	Unconditional stop, RNI @ m upon re-starting
IAI	53.(4+b)4	b	Add (A) to $(B^b) \rightarrow B^b$. Sign of B^b extended prior to addition
IAPR	77.57		Interrupt associated processor
IJD	02.4-7	m,b	If $(B^b) = 0$, RNI @ P + 1; if $(B^b) \neq 0$, $(B^b) - 1 \rightarrow B^b$, RNI @ m
IJI	02.1-3	m,b	If $(B^b) = 0$, RNI @ P + 1; if $(B^b) \neq 0$, $(B^b) + 1 \rightarrow B^b$, RNI @ m

*Trapped instruction if BDP module is not present in a system.

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDERSS FIELD	INSTRUCTION SYNOPSIS
INA	15.6	y	Increase (A) by y
INA, S	15.4	y	Increase (A) by y, sign of y is extended
INAC, INT	73*	ch	(A) is cleared and a 6-bit character is transferred from a peripheral device to the lower 6 bits of A
INAW, INT	74*	ch	(A) is cleared and a 12- or 24-bit word is read from a peripheral device into the lower 12 bits or all of A (word size depends on I/O channel)
INCL	77.50	x	Interrupt faults defined by x are cleared
INI	15.1-3	y, b	Increase (B^b) by y, signs of y and B^b are extended
INPC, INT, B, H	73**	ch, r, s	A 6- or 12-bit character is read from a peripheral device and stored in memory at a given location
INPW, INT, B, N	74.0**	ch, m, n	Word Address is placed in bits 00-14, 12- or 24-bit words are read from a peripheral device and stored in memory
INQ	15.7	y	Increase (Q) by y
INQ, S	15.5	y	Increase (Q) by y, sign of y is extended
INS	77.3	x, ch	Sense internal status if "1" bits occur on status lines in any of the same positions as "1" bits in the mask. RNI @ P + 1. If no comparison, RNI @ P + 2
INTS	77.4	c, ch	Sense for interrupt condition; if "1" bits occur simultaneously in interrupt lines and in the interrupt mask, RNI @ P + 1; if not, RNI @ P + 2
IOCL	77.51	x	Clears I/O channel or search/move control as defined by bits 00-07, 08, and 11 of x
ISA	77.674		Clear A and transfer (ISR) → A_{00-02} INSTRUCTION STATE REGISTER TO A
ISD	10.4-7	y, b	If (B^b) = y, clear B^b and RNI @ P + 2; if (B^b) ≠ y, (B^b) - 1 → B^b, RNI @ P + 1

*7-bit operation code, bit 17 in P = "1"
**7-bit operation code, bit 17 in P = "0"

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
ISE	04.0	y	If y = 0, RNI @ P + 2, otherwise RNI @ P + 1
ISE	04.1-3	y, b	If y = (B^b), RNI @ P + 2, otherwise RNI @ P + 1
ISG	05.0	y	If y $\geq$ 0, RNI @ P + 2, otherwise RNI @ P + 1
ISG	05.1-3	y, b	If $(B^b) \geq$ y, RNI @ P + 2, otherwise RNI @ P + 1
ISI	10.1-3	y, b	If (B^b) = y, clear B^b and RNI @ P + 2; if $(B^b) \neq$ y, $(B^b) + 1 \rightarrow B^b$, RNI @ P + 1
JAA	77.56		Transfer address of last executed jump → A
			JUMP ADDRESS TO A
JMP, HI A	67.5*		Jump
JMP, LOW A	67.7*		Jump
JMP, ZRO A	67.6*		Jump
LACH	22	r	(R) → A; load lower 6 bits of A
LCA, I	24	m, b	$(\overline{M}) \rightarrow A$
LCAQ, I	26	m, b	$(\overline{M}) \rightarrow A$, $(\overline{M + 1}) \rightarrow Q$
LDA, I	20	m, b	(M) → A
LDAQ, I	25	m, b	(M) → A, (M + 1) → Q
LDI, I	54	m, b	$(M_{00-14}) \rightarrow B^b$
LDL, I	27	m, b	(M) ∧ (Q) → A
LDQ, I	21	m, b	(M) → Q
LPA, I	37	m, b	(M) ∧ (A) → A
LQCH	23	r, 2	(R) → Q; load lower 6 bits of Q
MEQ	06.0-7	m, i	(B^1) - i → B^1; if (B^1) negative, RNI @ P + 1; if (B^1) positive, test (A) = (Q) ∧ (M); if true, RNI @ P + 2, if false, repeat sequence
MOVE, INT	72	c, r, s	Move c characters from r to s; $1 \leq c \leq 128_{10}$

*Trapped instruction if BDP module is not present in a system.

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
MTH	07.0-7	m, i	(B^2) - i → B^2; if (B^2) negative, RNI @ P + 1; if (B^2) positive, test (A) ≥ (Q) ∧ (M); if true, RNI @ P + 2; if false, repeat sequence
MUA, I	50	m, b	Multiply (A) by (M) → QA; lowest order bits of product in A
MUAQ, I	56	m, b	Multiply (AQ) by (M, M+1) → AQE
MVBF	64.1*	A, Ba, N1, C, Bc, N2	Move and blank fill
MVBF, D	64.1*	A, Ba, DC, C, Bc, N2	Move and blank fill
MVE	64.0*	A, Ba, N1, C, Bc, N2	Move
MVE, D	64.0*	A, Ba, DC, C, Bc, N2	Move
MVZF	64.2*	A, Ba, N1, C, Bc, N2	Move and zero fill
MVZF, D	64.2*	A, Ba, DC, C, Bc, N2	Move and zero fill
MVZS	64.3*	A, Ba, N1, C, Bc, N2	Move and zero suppress
MVZS, D	64.3*	A, Ba, DC, C, Bc, N2	Move and zero suppress
OSA	77.670		Clear A and transfer (OSR) → A_{00-02} OPERAND STATE REGISTER TO A
OTAC, INT	75**	ch	Character from lower 6 bits of A is sent to peripheral device, (A) retained
OTAW, INT	76**	ch	Word from lower 12 bits or all of A (depending on type of I/O channel) sent to a peripheral device

*Trapped instruction if BDP module is not present in a system
**7-bit operation code, bit 17 in P = "1"

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
OUTC, INT, B, H	75**	ch, r, s	Storage words assembled into 6 or 12-bit characters and sent to a peripheral device
OUTW, INT, B, H	76**	ch, m, n	Words read from storage to peripheral device
PAK	66.4*	A, Ba, N1, C, Bc	Pack
PAUS	77.0	x	Sense busy lines. If "1" appears on a line corresponding to "1" bits in x, do not advance P. If P is inhibited for longer than 40 ms, read reject instruction from P + 1. If no comparison, RNI @ P + 2
PFA	77.65	w	Clear A and transfer Page File index → A_{00-11} PAGE FILE TO A
PRP	77.61	x	Same as Paus (7760XXXX) except the real time clock is prevented from increment-int during the pause PRIORITY PAUSE
QEL	55.5		(Q) → E_L
QSE	04.7	y	If y = (Q), RNI @ P + 2, otherwise RNI @ P + 1; lower 15 bits of Q are used
QSE, S	04.5	y	If y = (Q), RNI @ P + 2, otherwise RNI @ P + 1. Sign of y is extended
QSG	05.7	y	If (Q) $\geq$ y, RNI @ P + 2, otherwise RNI @ P + 1
QSG, S	05.5	y	If (Q) $\geq$ y, RNI @ P + 2, otherwise RNI @ P + 1. Sign of y is extended
RAD, I	34	m, b	Add (M) to (A) → (M)
RCR	77.634		Transfer (Subcondition Register) → Condition Register. RESTORE CONDITION REGISTER
RIS	55.0		Use (ISR) in address relocation for operands RELOCATE TO INSTRUCTION STATE

*Trapped instruction if BDP module is not present in a system.
**7-bit operation code, bit 17 in P = "0"

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
ROS	55.4		Use (OSR) in address relocation for operands
			RELOCATE TO OPERAND STATE
RTJ	00.7	m	P + 1 → M (address portion) RNI @ m + 1, return to m for P + 1
SACH	42	r, 2	(A00-05) → R
SBA, I	31	m, b	(A) minus (M) → A
SBAQ, I	33	m, b	(AQ) minus (M, M + 1) → AQ
SBCD	77.72		Set BCD fault logic
SBJP	77.620		Transfers system from Monitor State to Program State when the next jump instruction is executed
			SET BOUNDARY JUMP
SBM	67.1*	A, Ba, N1, C, Bc, N2	Subtract
SCA, I	36	m, b	Where (M) contains a "1" bit, complement the corresponding bit in A
SCAN, J	65.4*	A, Ba, N2, SC, DC	Scan
SCAN, LR, EQ	65.0*	A, Ba, N2, SC, DC	Scan
SCAN, LR, NE	65.2*	A, Ba, N2, SC, DC	Scan
SCAN, RL, EQ	65.1*	A, Ba, N2, SC, DC	Scan
SCAN, RL, NE	65.3*	A, Ba, N2, SC, DC	Scan

*Trapped instruction if BDP module is not present in a system.

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
SCAQ	13.4-7	y, b	Shift (AQ) left end around until upper 2 bits of A are unequal. Residue K = k - shift count. If b = 1, 2, or 3, K → B^b; if b = 0, K is discarded
SCHA, I	46	m, b	(A00-16) → (M00-16)
SCIM	77.53	x	Selectively clear Interrupt Mask Register for each "1" bit in x. The corresponding bit in the Mask Register is set to "0"
SDL	77.624		Causes next LDA instruction to: 1. (M) → A 2. Store 77777777 @ M SET DESTRUCTIVE LOAD
SEL	77.1	x, ch	If channel ch is busy, read reject instruction from P + 1. If channel ch is not busy, a 12-bit function code is sent on channel ch with a function enable, RNI @ P + 2
SFPF	77.71		Set floating point fault logic
SHA	12.0-3	y, b	Shift (A). Shift count K = k + (B^b) (signs of k and B^b extended). If bit 23 of K = "1", shift right; complement of lower 6 bits equal shift magnitude. If bit 23 of K = "0", shift left; lower 6 bits equal shift magnitude. Left shifts end around; right shifts end off
SHAQ	13.0-3	y, b	Shift (AQ) as one register. Shift count K = k + B^b (signs of k and B^b extended). If bit 23 of K = "1", shift right and complement of lower 6 bits equal shift magnitude. If bit 23 of K = "0", shift left and lower 6 bits equal shift magnitude. Left shifts end around; right shifts end off
SHQ	12.4-7	y, b	Shift (Q), Shift count K = k + (B^b) (signs of k and B^b extended). If bit 23 of K = "1", shift right; complement of lower 6 bits equal shift magnitude. If bit 23 of K = "0", shift left; lower 6 bits equal shift magnitude. Left shifts end around; right shifts end off
SJ1	00.1	m	If Jump Key 1 is set, jump to m
SJ2	00.2	m	If Jump Key 2 is set, jump to m

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
SJ3	00.3	m	If Jump Key 3 is set, jump to m
SJ4	00.4	m	If Jump Key 4 is set, jump to m
SJ5	00.5	m	If Jump Key 5 is set, jump to m
SJ6	00.6	m	If Jump Key 6 is set, jump to m
SLS	77.70		Program stops if Selective Stop switch is on; upon restarting RNI @ P + 1
SQCH	43	r, l	(Q00-05) → R
SRA	77.630		Clear A and transfer (Subcondition Register) → A_{00-02}
			SUBCONDITION REGISTER TO A
SRCE, INT	71*	c, r, s	Search for equality of character c in a list beginning at location r until unequal character is found, or until character location s is reached; $0 \leq c \leq 63_{10}$
SRCN, INT	71**	c, r, s	Same as SRCE except search condition is for inequality
SSA, I	35	m, b	Where (M) contains a "1" bit, set the corresponding bit in A to "1"
SSH	10.0	m	Test sign of (m), shift (m) left one place, end around and replace in storage. If sign negative, RNI @ P + 2; otherwise RNI @ P + 1
SSIM	77.52	x	Selectively set Interrupt Mask Register for each "1" bit in x. The corresponding bit in the Mask Register is set to "1"
STA, I	40	m, b	(A) → (M)
STAQ, I	45	m, b	(AQ) → (M, M + 1)
STI, I	47	m, b	(B^b) → (M00-14)
STQ, I	41	m, b	(Q) → (M)
SWA, I	44	m, b	(A00-14) → (M00-14)
TAI	53.40-70	b	(A00-14) → B^b
TAM	53.42	v	(A) → v

*7-bit operation code, bit 17 in P + 1 = "0"
**7-bit operation code, bit 17 in P + 1 = "1"

3300 AND 3500 INSTRUCTION LIST (Cont'd)

MNEMONIC CODE	OCTAL OPERATION CODE	ADDRESS FIELD	INSTRUCTION SYNOPSIS
TIA	53.1-3	b	Clear (A), $(B^b) \rightarrow$ A00-14
TIM	53.(4+b)3	v, b	$(B^b) \rightarrow$ v00-14
TMA	53.02	v	(v) → A
TMAV	77.6100		Initiate memory request. If reply occurs within 5 usec. RNI@ P + 2; if not RNI@ P + 1. Storage address is (B^2) with (OSR) or zero appended TEST MEMORY AVAILABILITY
TMI	53.(0+b)3	v, b	(v00-14) → B^b
TMQ	53.01	v	(v) → Q
TQM	53.41	v	(Q) → v
TST	67.4*	A, Ba, N1	Test
UPAK	66.5*	A, Ba, N1, C, Bc	Unpack
USC	77.77		Unconditional stop. Upon restarting RNI @ P + 1
UJP, I	01.1-3	m, b	Unconditional jump to M
XOA	16.6	y	y ∨ (A) → A, no sign extension
XOA, S	16.4	y	y ∨ (A) → A, sign of y is extended
XOI	16.1-3	y, b	y ∨ $(B^b) \rightarrow B^b$
XOQ	16.7	y	y ∨ (Q) → Q, no sign extension
XOQ, S	16.5	y	y ∨ (Q) → Q, sign of y is extended
ZADM	67.2*	A, Ba, N1, C, Bc, N2	Zero and add
ZADM, D	67.2*	A, Ba, DC, C, Bc, N2	Zero and add

*Trapped instruction if BDP module is not present in a system.

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